Claims 3, 4, 5, 7 and 8 are also identified as being rejected in paragraph 5. However, only claims 1 and 6 have been addressed in the statement of the rejection that follows. Claim 3 is rejected later (paragraph 6) on a different ground. Claims 4, 5, 7 and 8 are not discussed further. It is further noted that claim 5 was indicated to be drawn to patentable subject matter in the earlier Office Action of February 24, 2005. Apparently there has been an error in the listing of the claims rejected.

From a reading of the Office Action and the circumstances described above, applicant concludes that the status of the claims is as follows. Claims 1 and 6 stand rejected under 35 U. S. C. § 102(b) as being anticipated by newly cited U.S. patent 6,295,240 (Choi). Claim 3 stands rejected under 35 U. S. C. § 103(a) as being unpatentable over Choi in view of Ikeda, of record. Claims 9 and 10 stand allowed. Claims 4, 5, 7 and 8 stand allowable subject to their presentation independent of rejected parent claims. This response is filed based on the above interpretation of the Office Action. If this interpretation is incorrect, it is respectfully requested that any subsequent Office Action rejection be made non-final.

Claims 1 and 3 through 10 have been rejected under 35 U. S. C. § 102(b) as being anticipated by newly cited U.S. patent 6,295,240 (Choi). The rejection is respectfully traversed. Claims 9 and 10 have been allowed. The Office Action has not identified elements in Choi that are applicable to subject matter recited in claims 3, 4, 5, 7 and 8, nor discussed these claims in the statement of the rejection. Withdrawal of the rejection of claims 3 through 5 and 7 through 10 is therefore appropriate and solicited.

Independent claim 1 recites, *inter alia*, the following:

> said connection gate circuit includes first and second gates connected in series between said pair of bit lines and said pair of I/O lines,

said first gate conducts in response to said sense amplifier activation signal, and

said second gate conducts in response to said column selection signal.

Fig. 2 of Choi has been relied upon for disclosing the elements recited in claims 1 and 6. Choi does not illustrate or disclose a connection gate circuit coupled between bit lines and input/output lines as required by the claims. The circuits 23 and 24 of Choi are coupled between the lines DB,/DB and the sense amplifier 22. The lines DB,/DB are described as input/output lines. Bit lines are not shown. Further, the circuits 23 and 24 of Choi are not connected in series between line DB, /DB and lines connected to a sense amplifier. Rather, the circuits are connected via a capacitor in parallel.

Independent claims 1 and 6 both recite that the first and second gate conducts (claim 1) or the connection gate circuit connects the bit lines to the I/O lines (claim 6) in response to activation of both the sense amplifier activation signal and the column selection signal. In contrast, circuits 23 and 24 of Choi disconnects DB,/DB from the sense amplifier lines (which are not I/O lines) in response to the SA_STROBE signal and the COLUMN_SELECT signals; that is, when these signals are activated transistors MP21 and MP22 are turned off.

As Choi lacks disclosure of the claimed elements discussed above, independent claims 1 and 6 and the claims dependent therefrom are not anticipated. Withdrawal of the rejection is believed warranted and respectfully solicited.

Claim 3 has been rejected under 35 U. S. C. § 103(a) as being unpatentable over Choi in view of Ikeda, of record. Ikeda has been relied upon for concluding that it would have been obvious to provide Choi with an equalization circuit. Ikeda has not been relied upon for teaching

the connection gate circuit requirements of parent claim 1, discussed above. Therefore, this rejection is respectfully traversed. Withdrawal of the rejection is solicited.

Allowance of the application is respectfully solicited. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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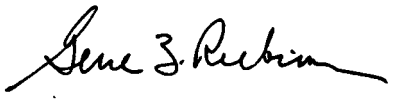

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